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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
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10/680,209

10/08/2003

Chih-Pin Hung

4459-133

7451

7590

10/06/2004

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EXAMINER

LEON, EDWIN A

ART UNIT

PAPER NUMBER

2833

DATE MAILED: 10/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

|                              |                        |  |                     |  |
|------------------------------|------------------------|--|---------------------|--|
| <b>Office Action Summary</b> | <b>Application No.</b> |  | <b>Applicant(s)</b> |  |
|                              | 10/680,209             |  | HUNG, CHIH-PIN      |  |
|                              | <b>Examiner</b>        |  | <b>Art Unit</b>     |  |
|                              | Edwin A. León          |  | 2833                |  |

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 02 July 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |                                                                                         |                                                                             |
|-----------------------------------------------------------------------------------------|-----------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)             | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____                                                |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____                                                             | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

### *Response to Amendment*

1. Applicant's amendment filed July 2, 2004 in which Claims 1-3 and 8 have been amended and new Claims 14-20 have been added has been placed of record in the file.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 14-15 and 17-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Centola et al. (U.S. Patent No. 6,633,490). With regard to Claims 1 and 14, Centola et al. discloses a package for electrically connecting to an external printed wiring board (100) and an external electronic device (110-1,2), the package comprising: a substrate (105-1) electrically connected to the external printed wiring board (100); a semiconductor chip (400) disposed on and electrically connected to the substrate (105-1); and a connector (115-1) disposed on the substrate (105-1) for electrically connecting

the semiconductor chip (400) to the external electronic device (110-1,2). See Figs. 3(a)-5.

With regard to Claim 8, Centola et al. discloses a package for electrically connecting to an external printed wiring board (100) and an external electronic device (110-1,2), the package comprising: a first substrate (105-1), a first semiconductor chip (400) electrically connected to the first substrate (105-1), a second substrate (105-2), a second semiconductor chip (400) electrically connected to the second substrate (105-2), a medium substrate (300) electrically connected to the first substrate (105-1) and the second substrate (105-2); and a connector (115-1) electrically connected to the first substrate (105-1) and the second substrate (105-2), wherein the first substrate (105-1) being electrically connected to the external printed wiring board (100) and the connector (115-1) being electrically connected to the external electronic device (110-1,2). See Figs. 3(a)-5.

With regard to Claim 15, Centola et al. discloses the substrate (105-1) having opposite upper and lower surfaces; the substrate (105-1) further comprising lower conductive elements (lower part of 500) on the lower surface thereof for electrically connecting the chip (400) to the external printed wiring board (100); the substrate (105-1) further comprising upper conductive elements (upper part of 500) on the upper surface thereof, the upper conductive elements (upper part of 500) being electrically connected to the chip (400) and the connector (115-1); and the chip (400) and the connector (115-1) being physically attached to different regions on the upper surface of the substrate (105-1). See Figs. 3(a)-5.

With regard to Claims 17 and 20, Centola et al. discloses the connector (115-1,2) having a shape of a box including an internal space (space inside aperture which receive contact from 110 and shown in Fig. 5) and an opening (aperture which receive contact from 110 and shown in Fig. 5) on a side of the box. See Figs. 3(a)-5.

With regard to Claim 18, Centola et al. discloses the first substrate (105-1) being physically positioned above the medium substrate (300) and the connector (115-1), which, in turn, are physically positioned above the second substrate (105-2). See Figs. 3(a)-5.

With regard to Claim 19, Centola et al. discloses the first and second substrates (105-1,2) being physically separated by a gap (Fig. 4) and the chips (400) are positioned within the gap (Fig. 4). See Figs. 3(a)-5.

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 2-7, 9-13 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Centola et al. (U.S. Patent No. 6,633,490) in view of Lu et al. (U.S. Patent No. 6,294,731). Centola discloses the claimed invention as shown above except for the substrate comprising a plurality of solder balls or a plurality of pins, the connector

being disposed on and electrically connected to the substrate by a surface mount technology process, the semiconductor chip being electrically connected to the substrate by a wire bonding process, the semiconductor chip being electrically connected to the substrate by a flip chip technology process and a molding compound for encapsulating the semiconductor chip.

However, Lu et al. discloses a similar connector having the substrate (570) comprising a plurality of solder balls (typically found on the BGA, Column 9, Line 41) and being electrically connected to the semiconductor chip (512) for electrically connecting the semiconductor chip (512) to the external printed wiring board (598), the substrate (570) comprising a plurality of pins (Column 9, Lines 22-44) and being electrically connected to the semiconductor chip (512) for electrically connecting the semiconductor chip (512) to the external printed wiring board (598), the connector (550) being disposed on and electrically connected to the substrate (570) by a surface mount technology process (Column 9, Lines 22-44), the semiconductor chip (512) being electrically connected to the substrate (570) by a wire bonding process (Column 9, Lines 22-44), the semiconductor chip (512) being electrically connected to the substrate (570) by a flip chip technology process (Column 9, Lines 22-44) and a molding compound (530) for encapsulating the semiconductor chip (512). See Figs. 1-7.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify package of Centola et al. by having the substrate comprising a plurality of solder balls or a plurality of pins, the connector being disposed on and electrically connected to the substrate by a surface mount technology process,

the semiconductor chip being electrically connected to the substrate by a wire bonding process, the semiconductor chip being electrically connected to the substrate by a flip chip technology process and a molding compound for encapsulating the semiconductor chip as shown in Lu et al. in order to connect the parts of the package more effectively.

### ***Response to Arguments***

6. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edwin A. León whose telephone number is (571) 272-2008. The examiner can normally be reached on Monday - Friday 10:00-6:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paula A. Bradley can be reached on 571-272-2800, extension 33. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

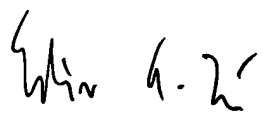
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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Gary Paumen  
Primary Examiner



Edwin A. Leon  
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EAL  
October 1, 2004